Birzeit University

Computer Systems Engineering Department

Computer Organization- ENCS 238

First Exam, May, 6, 2010

2nd semester, 2009/2010

(2 hours)

Section 1: Abdalkarim Awad **Section 2: Mohammad Abu- Ayyash**

Section 3: Aziz Qaroush

Name: **ID:**

Part One (True or False) (20Marks):

1	Given Ax=FFEE BX=7777 the instructions *cmp AX, BX* followed by *JGE L1* will change the IP to the value associated with L1 (i.e go to L1)	**F**
2	Hit ratio measures the expected probability of data being found in main memory.	**F**
3	Write-through cache reduces the number of write operations to main memory	**F**
4	Direct mapped, fully associative and set associative caches need block replacement algorithms	**F**
5	In the LRU (Least Recently Used) replacement algorithm, the data that has been in cache memory the longest time is replaced.	**F**
6	The access method used in EPROM is the Random Access	**T**
7	add *AL, [2000]* is illegal 8086 instruction	**F**
8	The instruction *mul Al, 20H* is illegal 8086 instruction	**T**
9	Both DRAM and SRAM need refresh	**F**
10	The instruction *Mov AX,[DX]* is a legal 8086 instruction	**F***

* DX, AX and CX can't be used as pointers to the data segment. We can us BX (i.e. Mov Ax,[BX] is legal)

Part Two (Assembly): (35 Marks)

1. Assembly languages are difficult for many reasons such as difficult to read, very difficult to debug, …. But still it has many advantages over high level languages. Give three of these advantages. (5 Marks)

   1 Assembly program size is smaller than high level languages
   2 Programs in assembly language will be executed faster than program in high level languages
   3 It access the hardware more efficient.

2. Write a complete assembly program that reads a key from the keyboard and if this key is a number then print on the screen the messages "A number has been pressed" else it print the messages "a non-number has been pressed". You may need the following information (10Marks)

```
.model small
.stack 100
.data
m1 db " A number has been pressed$"
m2 db " A non- number has been pressed$"
.code
mov ax,@data
mov ds,ax

mov ah,1
int 21h

cmp al,"0"
jb notnumber
cmp al,"9"
ja notnumber

lea dx,m1
mov ah,9
int 21h
jmp exit1

notnumber:
lea dx,m2
mov ah,9
int 21h

exit1:
mov ah,4ch
int 21h
end
```

   - ASCII codes for digits 0-9 are 30H-39H
   - For display use service 6H (i.e., AH=6H) of Int 21h (DOS interrupt), where the value to be displayed is placed in DL. Or service 2H (i.e., AH=2H) where the value to be displayed is placed in DL. And service 1H to read from the keyboard where the ASCII value of the inserted key will be in AL.

3. Assume(all values are in hex) (10 Marks)

AX=0000 BX=00050 CX=0003 DX=0000 SI=0050 DI=0000
CS=2000 SS=4000 DS=5000 ES=2000 SP=3000 BP=00050
IP=100

42FFF	12
43000	34
43001	56
43002	78
…	….

5004F	AA
50050	BB
50051	CC
50052	DD
…	…

```
Mov cx,7
L:
Inc DI
Loop L
or AX,[BX]      ;
Lea DX,[SI]     ;
POP SI
```

a. What is the physical address of the next instruction to be executed?

CS*10+IP
20000 +100=20100

b. What is the physical address of the source operand of the fourth instruction?

DS*10+BX
50000+50=50050

c. What is the new value of the affected registers after executing these instructions?

AX: CCBB CX:0000 DX:0050 SI:5634 DI:0007 SP:3002 IP:N/A

d. What is the physical address of the sources operand in the instruction mov DX,[BP+5]

SS*10+BP+5
40000+50+5=40055

Note that **SP & BP are two pointers associated with SS**. SP points to the top of stack, and BP points to any location we required in stack segment.

e. What is the SP and SS after the two instructions push AX push BX

SS:4000 SP 2FFE

4. Show how the AL and Flags are affected by (5 Marks)

```
Mov AL, 0BBH
ADD AL,0CCH
```

AL= 87 CF=1 OF=0 ZF=0 SF=1

5. Conditional jump (i.e JZ , JNZ…) allow relative range of only +127/-128 bytes form their current location. Knowing that unconditional jump does not have this limitation, show how to implement JZ L1 where L1 is located out side the +127/-128 range? (5 Marks)

```
JNZ skip
Jmp L1
```

Skip:

Part Three (Cache & Internal Memory): (45 Marks)

1. What is the performance advantage of using a write-back cache over a write-through cache? (4Marks)

2. Assume that we have 32-bit processor and it is byte-addressed (i.e. addresses specify bytes). Suppose that it has two way set-associative 512-byte cache, (16 bytes) cache lines (blocks), and uses LRU replacement.

   a. Split the 32-bit address into "tag", "set", and "word" pieces. Which address bits comprise each piece? (6 Marks)

# of words in each line = 16, need 4 bits to represent the word

# of lines = 512/16 = 32 lines

# of sets = # of lines/2 = 16, needs 4 bits to represent the set

The remaining bits of 32 bits used to represent Tag which is 32-4-4 = 24 bits

TAG: 24 bits	SET: 4 bits	W: 4 bits

   b. How many sets does this cache have? Explain. (3Marks)

   c. Below is a series of memory read references set to the cache from part (a). Assume that the cache is initially empty and classify each memory references as a hit or a miss. *Hint: start by splitting the address into components.* (12 Marks)

Address	Set Number	Hit/Miss?
0x007	*S0 / B0*	*M*
0x017	*S1 / B1*	*M*
0x104	*S0 / B1*	*M*
0x023	*S2 / B0*	*M*
0x203	*S0 / B0 LRU*	*M*
0x10F	*S0 /B1*	*H*

Address 007= 0 0 0 0 0 0 0 0 0 1 1 1

This means set 0 ⟹ 0 mod 16 = 0, (miss) we place this block in block 0 of the set 0 in the cache.

0X10F is hit, because this address and 0X104 address are found in the same block (same Tag "1").

d. Calculate the miss rate and hit rate. (5Marks)

Miss rate = 5/6

Hit rate= 1/6

3. Consider a system with cache, main memory and disk (or secondary memory) with the following parameters. It takes 10 ns to access cache, 100ns to access RAM and 10μs to access disk. The cache miss rate is 3% while miss rate in RAM is 20%. Estimate the average access time. (5Marks)

Ta = 0.97 * 10ns + 0.03(0.89 * 100ns + 0.11 * 10μs) =

97% of data is found in the cache.

3% of data is found out of the cache: 89% of this 3% data is in RAM, 11% in disk

(Note that access time is the "total time" to get the valid data. For example, RAM access time is the total time to get data from RAM including checking the cache)

4. Consider 8-bit processor that requires 64 Kbytes main memory. Design memory module for the processor using only 8 Kbytes memory chips organized as 16K X 4 bit. Draw your design. (10 Marks)

Solution:

- **Memory locations = 64 K locations, 16 address lines are needed (A0 – A15)**
- **Available chips 8 Kbytes (16K X4), we need 8 chips, each needs 14 (A2 –A15) address lines.**
- **The memory modules organized as four groups (banks) each contains two chips.**
- **A0 & A1 used to select one of the four groups. Use 2-to-4 decoder**